

Implementation of CMOS flexible fuzzy logic controller chip in current mode

Kazem Gheysari*, Behboud Mashoufi

Microelectronics Research Laboratory of Urmia University, Urmia, CO 57153, Iran

Received 25 August 2009; received in revised form 6 June 2011; accepted 7 June 2011

Available online 17 June 2011

Abstract

In this Paper, we implement multi-input Ordered Weighted Averaging operator in current mode and standard CMOS process, for the first time. For multi-input aggregation purpose, most part of our proposed circuit remains unchanged. Our circuit gives us a new class of Flexible Structured Fuzzy Logic Controller Chip (FS-FLC). We simulate our proposed circuit by HSPICE software in 0.35 μm process. Simulation results show that this aggregation operator has better behavior than conventional aggregation operator in the fuzzy logic controller chip for aggregation problem.

Crown Copyright © 2011 Published by Elsevier B.V. All rights reserved.

Keywords: Analog CMOS implementation; Current mode; Fuzzy logic controller chip; Ordered Weighted Averaging operator; Fuzzy aggregation operator; Fuzzy hardware

1. Introduction

Yager [2] introduced the Ordered Weighted Averaging operator to provide a method for aggregating multi-inputs that lie between max and min operators. The OWA operator provides a general class of parameterized aggregation operators that include the min, max, median operators. It is also useful for modeling different kinds of aggregation problems [3]. The researchers propose many extensions and applications in the areas of decision making, expert systems, data mining, approximate reasoning, fuzzy system and fuzzy control, neural network [4–9]. This operator is in the class of mean operators, it is idempotent, monotonic and commutative. The OWA aggregation operators allow us to adjust the degree of “anding” and “oring” easily and implicitly in an aggregation stage. Furthermore, their structure admits easy semantic interpretation using linguistic quantifiers [1,10]. Using these operators, we can allow a decision making to specify linguistically their agenda to aggregate a collection of criteria and then provide a formal implementation of this agenda.

Yager [11] provided a significant generalization of the Mamdani fuzzy logic controller structure. They called it, *Flexible Fuzzy Logic Controller (FS-FLC)*. Fig. 1 shows the structure of FS-FLC. With these types of controllers they provided for a parameterization of the basic operations used in the Mamdani type controller. More especially the operators used to implement the aggregation of antecedents in rules, the firing of rules, the aggregation of the rule outputs, and the defuzzification process are allowed to be variable. By parameterizing the aggregation operators

* Corresponding author. Tel.: +98 9354382544; fax: +98 4413452807.

E-mail addresses: st_k_gheysari@urmia.ac.ir, kgheysari@gmail.com (K. Gheysari).

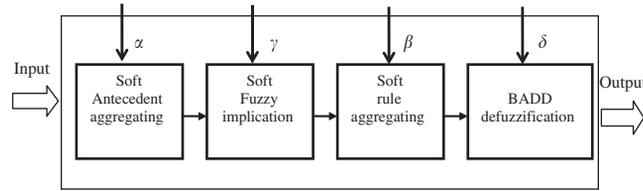


Fig. 1. Structure of Flexible Fuzzy Logic Controller.

we enable a higher degree of modeling for the system. They showed that the classic Mamdani model as well as the Takagi-Sugeno[12] become special case of this general class of models.

In [13] Yager and Filev introduced parameterized families of OWA operators, which they called S-OWA operators.

In this paper, we present CMOS implementation of multi-input S-OWA operator in 0.35 μm CMOS process Our design can be used in fuzzy logic controller chip for increasing the flexibility of fuzzy logic controller instead of min or max operator for aggregation problem, so we can access a flexible fuzzy logic controller chip [18,19].

The structure of this paper is as follows. Section 2 briefly reviews the Ordered Weighted Averaging operator. S-OWA operator is discussed in Section 3. Section 4 describes the CMOS implementation of S-OWA operator. Multi-Input S-OWA Operator is described in Section 5 and, the simulation results are presented in Section 6 and, finally conclusion is in Section 7.

2. Ordered Weighted Averaging operator

An OWA operator of dimension n is a mapping denoted $OWA_W = R^n \rightarrow R$ that has an associated n -dim vector $W = [w_1 \psi w_2 \dots \psi w_n]^T$ such that: [4,3]

$$w_i \in [0, 1]$$

$$\sum_i w_i = 1 \tag{1}$$

And where

$$F(a_1, a_2, \dots, a_n) = w_1 b_1 + w_2 b_2 + \dots + w_n b_n \tag{2}$$

where b_i is the i th largest element in the collection a_1, a_2, \dots, a_n . In particular the largest OWA operator results in the smallest “OR” operator *Max*, while the smallest in the largest “AND” operator *Min*. OWA operator provides an aggregation type operator that always lies between the “AND” and the “OR” aggregation.

$$I_{\max} = \max(I_1, I_2, \dots, I_n)$$

To accomplish this increase of flexibility, we shall use two ideas from the theory of fuzzy approximate reasoning, which were recently developed [8]. The first of them is the S-OWA aggregating operators [13] derived from the OWA aggregating operators originally introduced by Yager [2]. The second concept is the use of the Basic Defuzzification Distribution (BADD) [14] as a general tool for defuzzification of fuzzy sets.

3. S-OWA operators

It is noted that different OWA operators are distinguished by their weighting functions [15,3]. Yager and Filev [15] introduced parameterized families of OWA operators which they called S-OWA operators. The S-OWA operators are defined as:

S-OWA-OR (OR-like) aggregating operator (\tilde{V}):

$$\tilde{V}_i a_i = (1 - \beta) \frac{1}{m} \sum_{i=1}^m a_i + \beta V_i a_i \tag{3}$$

S-OWA-AND (AND-like) aggregating operator ($\tilde{\wedge}$):

$$\tilde{\wedge}_i a_i = (1 - \alpha) \frac{1}{m} \sum_{i=1}^m a_i + \alpha \wedge_i a_i \tag{4}$$

S-OWA-PRODUCT (Product-like) aggregating operator ($\tilde{\prod}$):

$$\tilde{\prod}_i a_i = (1 - \alpha) \frac{1}{m} \sum_{i=1}^m a_i + \alpha \prod_i a_i \tag{5}$$

In the above a_1, \dots, a_m are m objects that are aggregated and $0 \leq \alpha \leq 1, 0 \leq \beta \leq 1$.

Using the S-OWA-AND, S-OWA-OR operators, we can replace the conventional AND and OR operators used in the conventional Mamdani method. These replacements that are in the spirit of softening the aggregation operations provide a generalization of the operations.

Replacing the simple AND used to connect the antecedents in the individual rules with an S-OWA-AND operator. The logical connective AND is used to connect the antecedents in the individual rules. This connective is usually interpreted by the MIN aggregating operator:

$$F(a_1, a_2, \dots, a_n) = \beta \text{Min}_i(a_i) + \frac{1}{n}(1 - \beta) \sum_i (a_i) \tag{6}$$

Similarly, for S-OWA-OR operator we have

$$F(a_1, a_2, \dots, a_n) = \alpha \text{Max}_i(a_i) + \frac{1}{n}(1 - \alpha) \sum_i (a_i) \tag{7}$$

Therefore, these operators allow easy adjustment of the degree of ‘anding’ and ‘oring’ embedded in the aggregation by α and β parameters. We note that for $\alpha = 0$ the strength of firing is obtained as the arithmetic mean of the satisfactions of each of the antecedents, and for $\alpha = 1$, we receive the expression of the strength of firing used in the original Mamdani model.

For two fuzzy sets A and B we have

$$\mu_{A \cup B}(x) = \alpha \times \max(\mu_A, \mu_B) + \frac{(1 - \alpha)}{2}(\mu_A + \mu_B) \tag{8}$$

$$\mu_{A \cap B}(x) = \alpha \times \min(\mu_A, \mu_B) + \frac{(1 - \alpha)}{2}(\mu_A + \mu_B) \tag{9}$$

Parameter α sets with the defined bits in our CMOS implementation of S-OWA operators. These bits can be defined by a set of switches or by an external memory. These bits are inputs of the multiplier and divider circuits.

4. Analog CMOS implementation of Ordered Weighted Averaging operator

The nature of fuzzy variable systems requires extensive parallelism which makes analog circuits well appropriate to proceed high-speed numerous inferences and also limits the problem of error accumulation. The CMOS implementation of fuzzy logic controllers (FLC) performs in two modes of voltage and current [16]. It turns out that current mode is a practical choice for the input–output interface requirements of these circuits [16] and current-mode method is a reliable implementation of fuzzy logic architecture [17,36]. These current-mode basic logic cells exhibit good linearity which cannot be easily achieved in voltage-mode, and lead to fuzzy integrated systems that are globally smaller than in voltage-mode [18,19], then we selected current mode for implementation of S-OWA.

Fig. 2 shows the block diagram of the proposed circuit for multi-input S-OWA-AND operator in current mode. There are n -current mirror and scale factor circuit in the first stage of this block diagram. These blocks mirror input currents (I_1, I_2, \dots, I_n) at the output branches. The current mirror and scale factor circuit has two output currents. One of these currents goes to the MIN circuit is equal with input current but another one is I_i/n , where n is the number of input of S-OWA operator. MIN circuit finds the minimum current between its input currents ($I_1, I_2, I_3, \dots, I_n$). After MIN

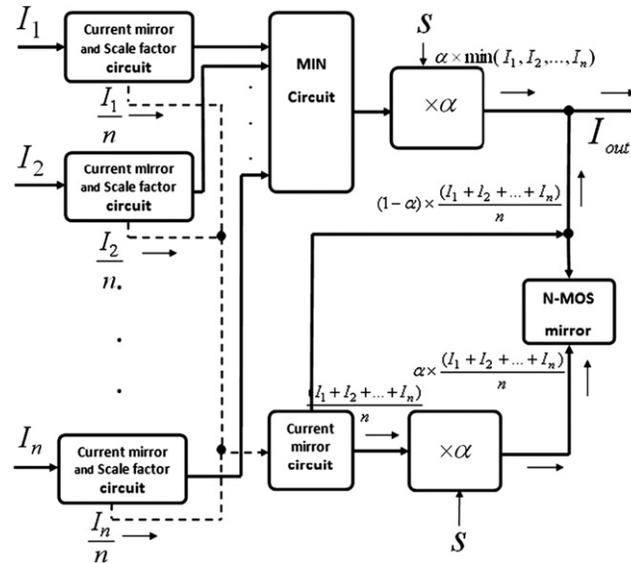


Fig. 2. Block diagram of the proposed multi-input S-OWA-AND Operator Circuit. This circuit uses multiplier and divider circuits in the $\times \alpha$ block.

circuit, there is multiplier and divider circuit ($\times \alpha$) which multiplies the minimum current with parameter α . Digital word S specifies the parameter α . Before the current mirror circuit block, outputs of first blocks are connected to each other to sum the second output current of first blocks. So, input current of the current mirror circuit is $(I_1 + I_2 + I_3 + \dots + I_n)/n$. There is multiplier and divider circuit ($\times \alpha$) after current mirror circuit which multiplies $(I_1 + I_2 + I_3 + \dots + I_n)/n$ with parameter α . There is $1 - \alpha$ in the main formula of S-OWA-AND operator, so we change the direction of current with N-MOS current mirror. Finally, we have the desired output current as follows:

$$I_{out} = \alpha \times \min(I_1, I_2) + \frac{(1 - \alpha)}{2}(I_1 + I_2) \tag{10}$$

4.1. Current mirror and scale factor circuit

Current mirror and scale factor circuit takes the input current and then produces two current (I_i and I_i/n), where n is the number of input of S-OWA operator and I_i is input current. I_i goes to the MIN circuit and I_i/n goes to the summation node before the current mirror circuit. Fig. 3 shows the circuit of current mirror and scale factor circuit.

4.2. MIN and MAX circuit

MIN circuit finds the minimum current between its input currents ($I_1, I_2, I_3, \dots, I_n$). We can select another desirable architecture for MIN circuit to achieve our desirable properties. For achieving S-OWA-OR, the MIN circuit must be replaced by MAX circuit.

Current-mode max operators are less costly to implement than min circuits [16]; therefore, MAX operator is implemented, then MIN operator is achieved by following equations:

$$\min(x_i) = \overline{\max(\overline{x_i})} = x_{ref} - \max(x_{ref} - x_i) \tag{11}$$

Or in current mode,

$$\min(I_i) = \overline{\max(\overline{I_i})} = I_{ref} - \max(I_{ref} - I_i) \tag{12}$$

We select $10 \mu A$ for I_{ref} . We use multi-inputs maximum circuit in [16]. Subtracting the current from I_{ref} in current mode is very simple. Fig. 4 shows the MAX circuit.

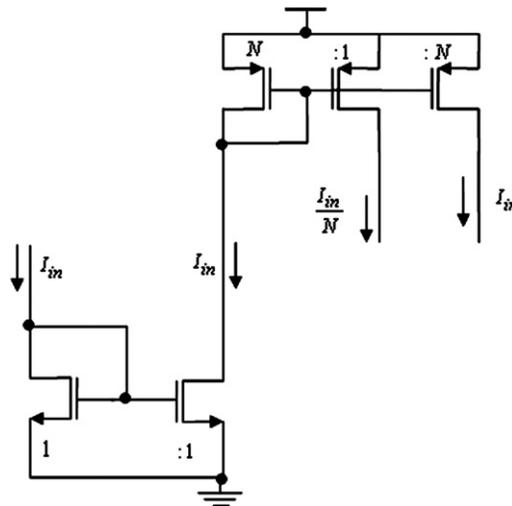


Fig. 3. Input current mirror and Scale factor circuit.

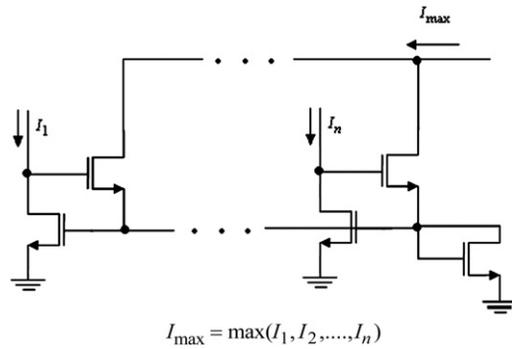


Fig. 4. MAX Circuit.

4.3. Multiplier and divider circuit

Multiplier and divider circuits are usually required in the fields of analog signal processing and parallel computing neural or fuzzy systems. Several techniques to design multiplier/divider circuits have been proposed in the literature. Conventional log–antilog or bipolar translinear techniques have been employed in the analog fuzzy chips described in [20,21]. These structures can be realized with CMOS technology by using MOS transistors working in subthreshold region. However, the low current levels make them operate slowly [22]. Low operating speed is also the main limitation of multiplier/dividers based on the time-division technique [23]. The MOS translinear principle is another approach. In this case, the main limitation is a low resolution because the performance of the resulting circuits is very sensitive to deviations from the simple square-law model of the transistors in saturation, caused by length-channel modulation, mobility reduction or mismatching [16,25,26]. Another technique widely employed is to invert the behavior of a multiplier by using local feedback or by inserting it in the feedback path of an inverting amplifier.

The performance of these multiplier/dividers depends primarily on the performance of the multiplier and the amplifier employed. Precision is mainly limited by offsets associated with the input and output variables [16,24,27]. The analog fuzzy chips reported in [28,29] contain these types of multiplier/dividers.

In the most reported CMOS divider circuits, transistors operate in weak inversion mode, consequently those divider circuits exhibit poor transient performances. On the other hand, some implementations of dividers in strong inversion mode feature a complex signal interface. For instance, in [29] a current-input voltage-output divider is presented.

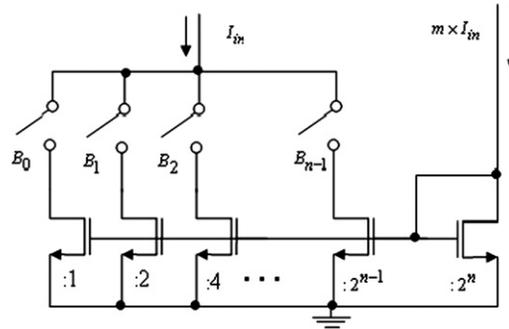


Fig. 5. Divider Circuit.

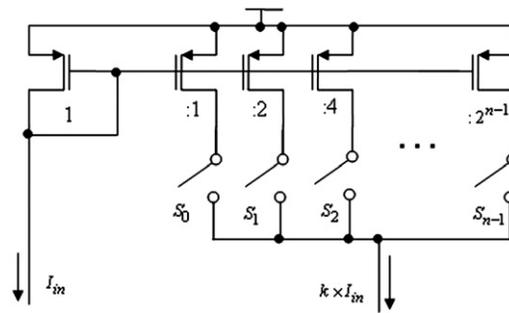


Fig. 6. Multiplier Circuit.

It needs an additional fully differential current-to-voltage converter at one of the divider inputs. In [30], another current-input current-output divider is proposed. In this device, one input current must be supplied twice to two different nodes of the circuit, while the other input is a floating current source. In digitally programmable Zero-Order TS's controllers, a typical approach for implementing the consequent singletons of the rules consists of using current-mode D/A converters.

In our design, the parameter α is defined by the two sets of switches. The states of switches S_0, S_1, \dots, S_{n-1} define the multiplication factor (k) and the switches B_0, B_1, \dots, B_{n-1} define the division factor (m). We can use Eqs. (13) and (14) for k and m , respectively.

$$k = (S_0 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + \dots + S_{n-1} \cdot 2^{n-1}) \tag{13}$$

$$m = \frac{(B_0 + B_1 \cdot 2^1 + B_2 \cdot 2^2 + \dots + B_{n-1} \cdot 2^{n-1})}{2^n} \tag{14}$$

Then

$$k \geq 1, \quad 0 < m < 1$$

$$\alpha = k \times m, \quad 0 < \alpha < 1$$

Figs. 5 and 6 show the divider circuit and multiplier circuit, respectively. The principles of operation of the multiplier and divider circuits are same and we multiply or divide the input current by changing the aspect ratio (W/L) of the transistors. In here, we briefly describe the principle of operation of multiplier circuit. More description can be found in [31].

In Fig. 6, the transistors have a aspect ratio of either (W/L) = 1, (W/L) = 2, (W/L) = 4, ..., (W/L) = 2^{n-1} . In this way, the current produced at the different output branches is progressively multiplied by a factor of 2. In standard applications, this circuit is usually used, thus providing a set of binary-weighted currents, which can be controlled

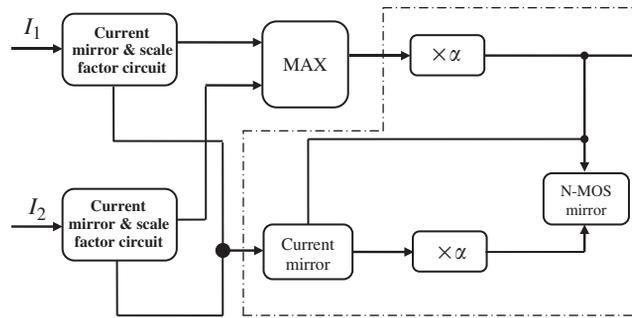


Fig. 7. Two input S-OWA-OR operator circuit.

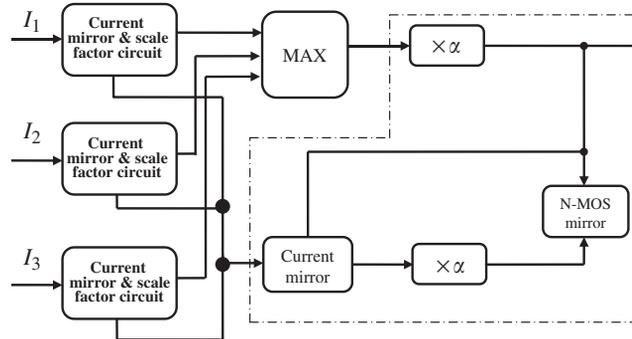


Fig. 8. Three input S-OWA-OR operator circuit.

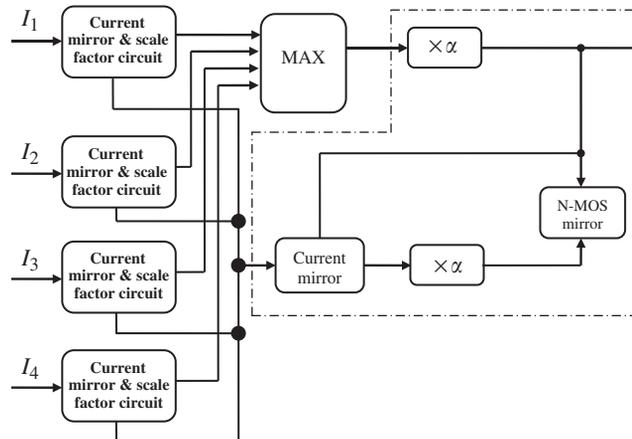


Fig. 9. Four input S-OWA-OR operator circuit.

digitally by means of switches to produce any combination of them. We can improve this circuit by using a decoder for setting of the switches. In this way, a digital word specifies the connected or opened switches.

5. Multi-input S-OWA operator in CMOS

In this section, we consider multi-input S-OWA operator circuit. We want to survey the limitations and advantages of our proposed circuit for input more than two because one of the important issues to consider while designing fuzzy

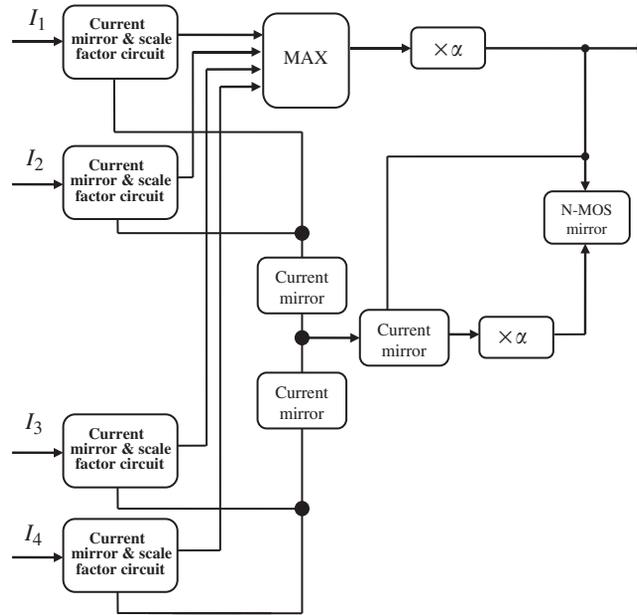


Fig. 10. Decreasing the input capacitor of the nodes before the current mirror for obtaining high-speed OWA operator circuit.

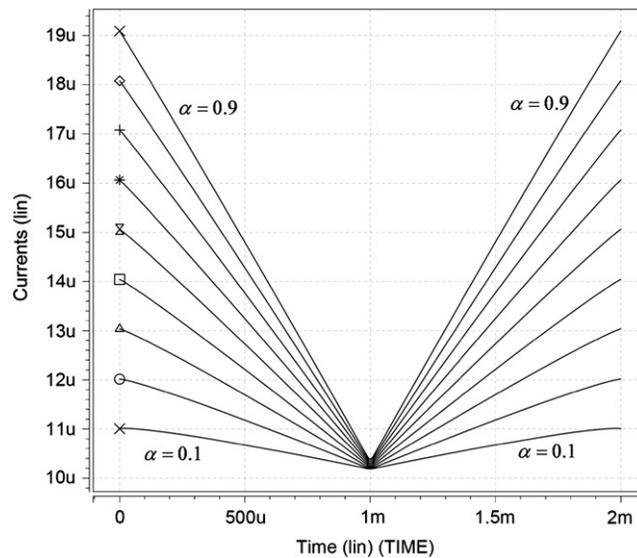


Fig. 11. Simulation results of two input S-OWA-OR operator for linear changes I_1 from $20 \mu\text{A}$ to 0 and I_2 from 0 to $20 \mu\text{A}$ and α from 0.1 to 0.9.

aggregation circuit is the complexity of the circuit as a function of the number of inputs N . A naive approach to design an N -input T -Norm or T -CoNorm consisting in building a binary tree by cascading 2-input operators [32,33]. However, while the complexity of the circuit is $O(2N-1)$, the total input–output delay grows proportionally to $\log_2(N)$ [34]. In [35], a method to avoid binary trees, Multi-Input T -Norm (MIN) and T -CoNorm (MAX) operators, is suggested, but the proposed topologies have $O(N^2)$ complexity. Whereas the input capacitance at each input is proportional to the number of inputs N ; so, when N becomes large enough, the performance in terms of circuit sizes, current consumption and total delay decrease, compared with a binary tree with the same number of inputs. Three main criterions should be taken into account while designing these operators are: (1) Parallelism: cascading unit cells should be avoided and the

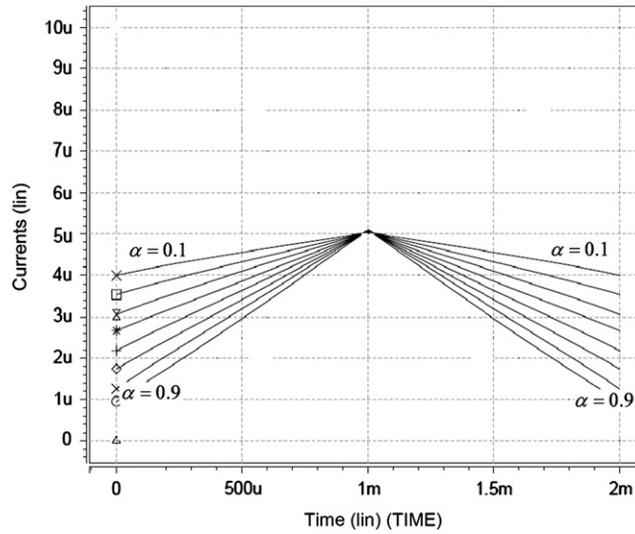


Fig. 12. Simulation results of two input S-OWA-AND operator for linear changes I_1 from 10 μ A to 0 and I_2 from 0 to 10 μ A and α from 0.1 to 0.9.

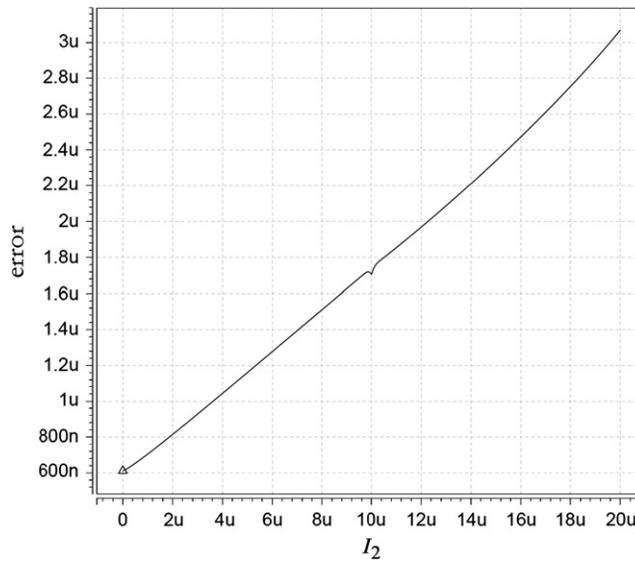


Fig. 13. Error between ideal output and output of simulation of S-OWA-OR operator circuit for $I_1 = 10 \mu$ A and I_2 increases from 0 to 20 μ A and $\alpha = 0.6$.

same input-output delay obtained from every circuit input. (2) Input transparency: each input circuit must represent the same load to any input signal, independently of N . (3) $O(N)$ complexity: the size and the current consumption of the circuit should be proportional to the number of inputs N .

Figs. 7–9 show that block diagram of S-OWA-OR for two inputs and three inputs and four inputs, respectively. One of the most important properties of our proposed circuit is that for more than two inputs OWA, most parts of circuit remain unchanged, in other words when the number of inputs of OWA circuit increases, there are not many changes in the circuit complexity. Dashed lines in Figs. 7–9 show the unchanged parts of S-OWA-OR circuit.

A problem of the proposed design is the input capacitor of the node, before of the current mirror. This capacitor gets very large for more than two inputs and it affects the speed of OWA operator in analog fuzzy logic controller chip, but we can decrease this capacitor by using hierarchical design as shown in Fig. 10.

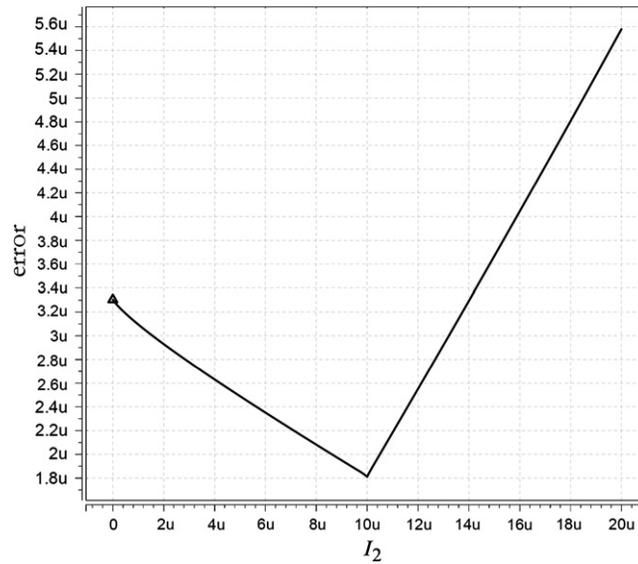


Fig. 14. Error between ideal output and output of simulation of S-OWA-OR operator circuit for $I_1 = 10 \mu\text{A}$ and I_2 increases from 0 to $20 \mu\text{A}$ and $\alpha = 0.1$.

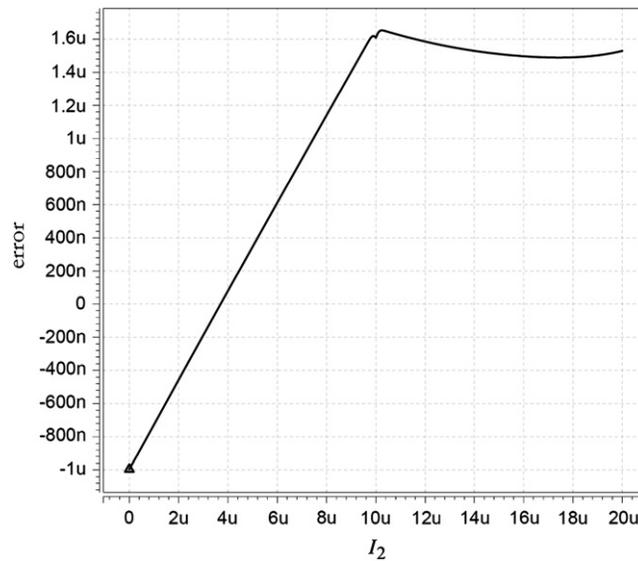


Fig. 15. Error between ideal output and output of simulation of S-OWA-OR operator circuit for $I_2 = 10 \mu\text{A}$ and I_1 increases from 0 to $20 \mu\text{A}$ and $\alpha=0.9$.

6. Simulation results

Several simulation cases were conducted to assess the performance of the proposed fuzzy aggregation operator circuit. We simulated S-OWA operator circuit for two input and different α and we compared simulation results with ideal results. Then, we simulated three inputs and four inputs S-OWA operator and compared these different architectures.

Fig. 11 shows the simulation results of two input S-OWA-OR operator for linear changes of I_2 from $20 \mu\text{A}$ to zero and I_1 from zero to $20 \mu\text{A}$ and for $\alpha = 0.1, 0.2, \dots, 0.9$. In another simulation, we simulated two input S-OWA-AND operator for linear changes I_2 from $10 \mu\text{A}$ to zero and I_1 from zero to $10 \mu\text{A}$ and α from 0.1 to 0.9. Fig. 12 shows its results.

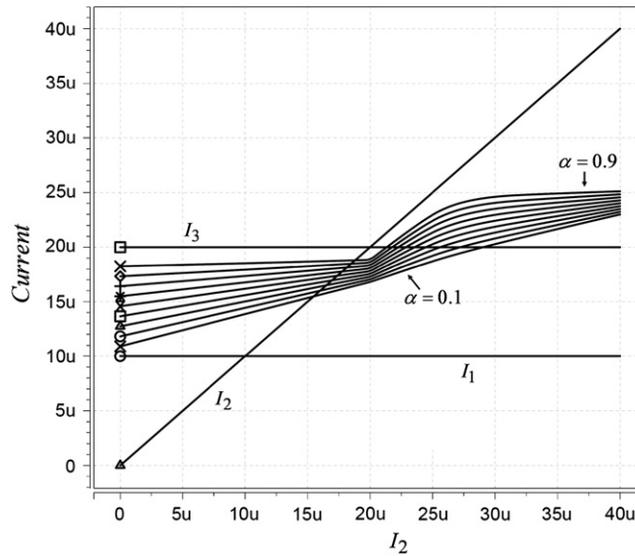


Fig. 16. Simulation results of three input S-OWA-OR operator circuit for $I_1 = 10 \mu\text{A}$, $I_3 = 20 \mu\text{A}$, I_2 varies from 0 to 40 μA and $\alpha = 0.1, 0.2, \dots, 0.9$.

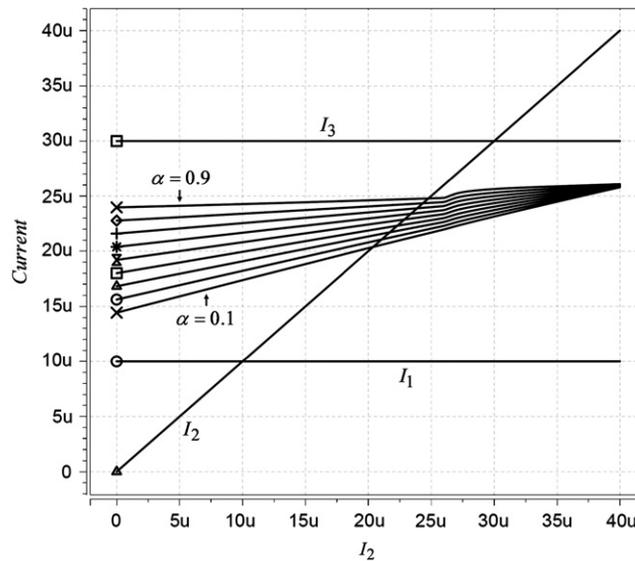


Fig. 17. Simulation results of three input S-OWA-OR operator circuit for $I_1 = 10 \mu\text{A}$ and $I_3 = 30 \mu\text{A}$ and I_2 varies from 0 to 40 μA and $\alpha = 0.1, 0.2, \dots, 0.9$.

We considered the precision of the proposed circuit in next simulations. In these simulations, we calculated the error between ideal output and output of simulation result of S-OWA-OR operator for different α . Fig. 13 shows the error between ideal output and output of simulation result of two input S-OWA-OR operator for $\alpha = 0.6$. Fig. 13 shows that for $\alpha = 0.6$ there is a linear relationship between input current and output error; in other words, in $\alpha = 0.6$, if we increase the input current, the difference between ideal output and output of simulation result will increase. Fig. 14 shows the error between ideal output and output of simulation for $\alpha=0.1$. When I_1 is larger than I_2 , the error decreases and when I_2 is bigger than I_1 , the error increases. The difference is larger between ideal output and output of simulation results of S-OWA-OR operator for $\alpha = 0.1$ than $\alpha = 0.6$ and 0.9. Fig. 15 shows the error between ideal output and output of simulation result of S-OWA-OR operator for $\alpha = 0.9$. In Fig. 15, When I_1 is bigger than I_2 , the error increases and when I_2 is bigger than I_1 , the error remains constant, approximately.

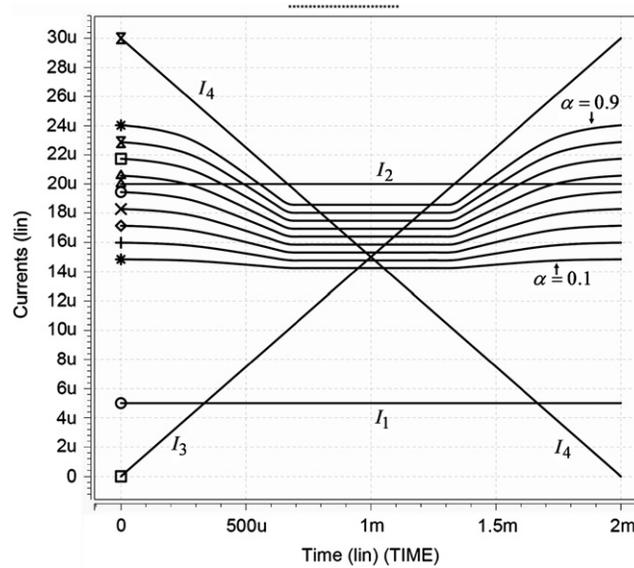


Fig. 18. Simulation results of four input S-OWA-OR circuit for $I_1 = 5 \mu\text{A}$, $I_2 = 20 \mu\text{A}$, I_3 varies from 0 to $30 \mu\text{A}$ and I_4 varies from $30 \mu\text{A}$ to 0 and $\alpha = 0.1, 0.2, \dots, 0.9$.

In another simulation, we simulate three inputs S-OWA-OR circuit. Fig. 16 shows the simulation results when I_2 varies from 0 to $40 \mu\text{A}$ and $I_1 = 10 \mu\text{A}$ and $I_3 = 20 \mu\text{A}$ and $\alpha = 0.1-0.9$ and Fig. 17 shows the simulation results when I_2 varies from 0 to $40 \mu\text{A}$ and $I_1 = 10 \mu\text{A}$ and $I_3 = 30 \mu\text{A}$ and $\alpha = 0.1-0.9$. Fig. 18 shows the simulation results for four input S-OWA-OR operator circuit when $I_1 = 5 \mu\text{A}$ and $I_2 = 20 \mu\text{A}$ and I_3 varies from 0 to $30 \mu\text{A}$ and I_4 varies from $30 \mu\text{A}$ to 0 and $\alpha = 0.1-0.9$.

7. Conclusion

Multi-input Ordered Weighted Averaging (OWA) operator is implemented in CMOS technology for the first time. This circuit can be used in fuzzy logic controller chip for aggregating purpose instead of MIN/MAX circuit, so we have a flexible fuzzy logic controller chip (FS-FLC). The proposed FS-FLC chip can be programmed by two sets of switches. The proposed circuit for number of inputs more than two does not have much change and its complexity as a function of the number of inputs is lower than last approaches. For big α , the error between output of simulation result and ideal output is low.

Acknowledgments

The authors would like to thank the Ph.D. students of microelectronics research laboratory of Urmia University and Sharif University of technology for their kind helpful assistances.

References

- [1] L. Zadeh, A computational approach to fuzzy quantifiers in natural languages, *Computing and Mathematics with Applications* 9 (1983) 149–184.
- [2] R.R. Yager, On ordered weighted averaging aggregation operator in multicriteria decisionmaking, *IEEE Transactions on Systems, Man, and Cybernetics* 18 (1) (1988) 183–190.
- [3] X. Liu, Some properties of weighted average operator, *IEEE Transactions on Systems, Man, and Cybernetics—Part B* 36 (1) (2006) 118–127.
- [4] R.R. Yager, J. Kacprzyk, *The Ordered Weighted Averaging Operators—Theory and Applications*, Kluwer, Norwell, MA, 1997.
- [5] E. Herrera-Viedma, O. Cordon, M. Luque, A.G. Lopez, A.M. Munoz, A model of fuzzy linguistic IRS based on multi-granular linguistic information, *International Journal of Approximate Reasoning* 34 (2003) 221–239.
- [6] R.R. Yager, Connectives and quantifiers in fuzzy sets, *Fuzzy Sets Systems* 40 (1991) 39–75.

- [7] R.R. Yager, On a semantics for neural networks based on fuzzy quantifiers, *International Journal of Intelligent Systems* 7 (1992) 765–786.
- [8] R.R. Yager, D.P. Filev, Fuzzy logic controllers with flexible structures, *Proceedings of the 2nd International Conference on Fuzzy Sets and Neural Networks*, Tizuka, 1992, pp. 317–320.
- [9] V. Torra, OWA operators in data modeling and reidentification, *IEEE Transactions on Fuzzy Systems* 12 (5) (2004) 652–660.
- [10] L. Zadeh, A fuzzy sets, *Information and Control* 8 (1965) 338–356.
- [11] R.R. Yager, D.P. Filev, T. Sadeghi, Analysis of flexible structured fuzzy logic controllers, *IEEE Transactions on Systems, Man, and Cybernetics* 24 (7) (1994) 1035–1043.
- [12] T. Takagi, M. Sugeno, Fuzzy identification of systems and its application to modeling and control, *IEEE Transactions on Systems, Man, and Cybernetics* 15 (1985) 116–132.
- [13] R.R. Yager, D.P. Filev, Parameterized “andlike” and “orlike” OWA operators,” Technical Report 1216, Machine Intelligence Institute, Iona College, 1992.
- [14] D.P. Filev, R.R. Yager, A generalized defuzzification method under BAD distributions, *International Journal of Intelligent Systems* 6 (1991) 687–697.
- [15] R.R. Yager, D.P. Filev, Parametrized “andlike” and “orlike” OWA operators, *International Journal of General Systems* 22 (1994) 297–316.
- [16] I. Baturone, S. Sanchez-Solano, A. Barriga, J.L. Huertas, Implementation of cmos fuzzy controller as mixed-signal integrated circuits, *IEEE Transactions on Fuzzy Systems* 5 (1) (1997) 1–19.
- [17] L. Lemaite, M.J. Patyra, D. Mlynek, Analysis and design of CMOS fuzzy logic controller in current mode, *IEEE Journal of Solid-State Circuits* 29 (3) (1994) 317–322.
- [18] K. Gheysari, A. Khoei, Kh. Hadidi, M. Mokarram, Analog CMOS implementation of order weight average operator for fuzzy logic controller chip, in: *IEEE International Conference of Intelligent System (IS 2008)*, Varna, Bulgaria, 6–8 September, 2008, pp. 22–25.
- [19] K. Gheysari, A. Khoei, Kh. Hadidi, N. Kamali, Low noise CMOS implementation of order weight average operator for fuzzy logic controller chip, in: *20th IEEE International Conference on Microelectronics (ICM)—Circuits and Systems*, 14–17 December 2008, Sharjah, UAE, pp. 33–38.
- [20] T. Kettner, K. Schumacher, K. Goser, Realization of a monolithic fuzzy logic controller, *Proceedings of the ESSCIRC Sevilla (1993)* 66–69.
- [21] T. Yamakawa, A fuzzy inference engine in nonlinear analog mode and its application to a fuzzy logic control, *IEEE Transactions on Neural Networks* 4 (1) (1993) 496–522.
- [22] C.Y. Wu, J.F. Lan, CMOS current-mode neural associative memory design with on-chip learning, *IEEE Transactions on Neural Networks* (1996) 167–181.
- [23] A. Cichoki, R. Unbehauen, A novel switched-capacitor four-quadrant analog multiplier–divider and some of its applications, *IEEE Transactions on Instrumentation and Measurement* 35 (2) (1986) 156–162.
- [24] D.H. Sheingold, *Nonlinear circuit handbook*, Analog Devices, Inc., Norwood, Massachusetts, 1976.
- [25] R.J. Wiegink, *Analysis and synthesis of MOS translinear circuits*, Kluwer Academic Publisher, Boston, 1993.
- [26] C.Y. Chen, C.Y. Huang, B.D. Liu, Current-mode defuzzifier circuit to realize the centroid strategy, *IEE Proceedings. G* 144 (3) (1997) 265–271.
- [27] N.I. Kachab, M. Ismail, Linearization techniques for n th order sensor models in MOS VLSI technology, *IEEE Transactions on Circuits and Systems* 38 (12) (1991) 1439–1450.
- [28] O. Landolt, Efficient analog CMOS implementation of fuzzy rules by direct synthesis of multidimensional fuzzy subspaces, *Proceedings of the FUZZ-IEEE*, San Francisco, 1993, pp. 453–458.
- [29] J.L. Huertas, S.S. Solano, I. Baturone, A. Barriga, Integrated circuit implementation of fuzzy controllers, *IEEE Journal of Solid-State Circuits* 31 (7) (1996) 1051–1058.
- [30] K. Bult, H. Wallinga, A class of analog CMOS circuits based on the square law characteristic of a MOS transistor in saturation, *IEEE Journal of Solid-State Circuits* 22 (3) (1987) 357–365.
- [31] B. Razavi, *Design of Analog CMOS integrated circuit*, McGraw-Hill Publication, New York, 2001.
- [32] T. Yamakawa, T. Miki, The current mode fuzzy logic integrated circuits fabricated by the standard CMOS process, *IEEE Transactions on Computers* c-35 (2) (1986) 161–167.
- [33] S. Liu, S. Hwang, J. Tsay, CCII-based fuzzy membership function and MAX/MIN circuits, *IEE Electronics Letters* 29 (1) (1993) 116–118.
- [34] C. Dualibe, *Logique Floue: de la Théorie au Matériel*”, TFE Licence en Sciences Appliquées, Université catholique de Louvain, Louvain-la-Neuve, Belgium, September 1994.
- [35] M. Sasaki, T. Inoue, Y. Shirai, F. Ueno, Fuzzy multi-input maximum and minimum circuits in current mode and their analysis using bounded-difference equations, *IEEE Transactions on Computers* 39 (6) (1990) 768–774.
- [36] Gh. Yosefi, S. Aminifar, Sh. Neda, M.A. Daneshwar, Design of a mixed-signal digital CMOS fuzzy logic controller (FLC) chip using new current mode circuits, *AEU—International Journal of Electronics and Communications* 65 (3) (2011) 173–181.